

Session: Readout Electronics for next generation Liquid Scintillator Experiments

**“Physics opportunities of Large Liquid Scintillator Detectors”,
2nd Town Hall Meeting, Mainz, 14 October 2026**



Previous generation experiments

Borexino • 2007–21

Readout: gateless integrator, 8-bit FADC (Q + T)

Trigger: 20–30 hits in ~ 100 ns, 16 μ s gate

KamLAND/KamLAND-Zen) 2002–

Readout: ATWD waveforms, 128×1.5 ns, 3 gains

Trigger: NSum thresholds (prompt, delayed, burst)

Upgrade: MoGURA, dead-time-free FADC for post-muon neutrons

SNO • 1999–2006

Readout: custom ICs: sub-ns time, charge, 16-event analog memory

Trigger: analog sums of hits and charge (NHIT, ESUM)

Daya Bay • 2011–20

Readout: 40 MHz charge ADC + TDC

Trigger: NHIT ≥ 45 or ESUM ≥ 65 PE

Upgrade: 1 GS/s FADC for waveform reconstruction

Double Chooz • 2011–18

Readout: full waveforms, 500 MS/s, 8-bit

Trigger: analog sum $\times$ PMT-group multiplicity

Dead time zero, via paged memory

RENO • 2011– 2023

Readout: Super-K QBEE: charge-to-time + multi-hit TDC

Trigger: software on all hits

Current state-of-the-art large LS experiments

SNO+ (2018 →)

Kept SNO front-end cards: one charge and one time per hit

Upgraded: MTC/A+ trigger cards for scintillator currents; auto re-trigger beyond 400 ns

Readout: XL3 cards push each crate over Ethernet; CAEN V1720 digitizes trigger sums

JUNO (2025 →)

Large PMTs $17,612 \times 20''$: one underwater box per 3 PMTs with 1 GS/s ADC, FPGA and 2 GB supernova buffer

Trigger ~350 hits in 304 ns (~200 keV) at ~400 Hz; multi-messenger trigger at ~7 kHz

Small PMTs $25,600 \times 3''$: self-triggered CATIROC ASICs; ~13,000 of ~20,000 live channels used

DAQ ~40 GB/s in, under 500 Mbps out after online classification

JUNO-TAO · (2026 →)

Sensors: ~10 m² of SiPMs, ~4,000 tiles, operated at -50 °C

Readout: custom discrete front-end boards with two channels per tile, ~8,000 channels in total

Note: KLauS ASIC readout studied as an alternative, but discarded

KamLAND2-Zen · (2028? →)

Readout ~2,000 × 20" PMTs on 16-channel RFSoc boards: 1 GS/s high gain + 250 MS/s, 16-bit low gain to ~8 V

Trigger every waveform over 1 GbE to a software trigger; digital baseline restoration

Power 43 W per 16 channels, 56% better per channel than the previous boards

Requirements for future large LS experiments

- Very good energy resolution at the Q-value
- Background rejection using time coincidences and Cherenkov/Scintillation light separation
 - Ex., ^8B solar neutrinos rejection

Regardless of the increased LS target mass:

- Preserve light collection (photon statistics remains important)
- Perform high efficiency background rejection (T/Q, Cherenkov/Scintillation separation)
- Keep timing information (topological cuts, MSE/SSE)
- Aim for high reliability (large detectors require electronics close to the LS/water)
- Do we care about radiopurity of electronics and sensors for future $0\nu\beta\beta$ LS experiments?

Requirements

- High Speed ($\geq 1\text{GS/s}$) Waveform digitization seems to be the best option
- Digitize your signal very close to the source and transmit the digital packet over long distances ($\geq 100\text{ m}$)
- Use ASICs or commercially available ADCs, but add FPGA (and DDR memory) on boards for digital data processing
- Perform trigger validation, data reduction via software in real time
- Aim for a zero-deadtime system
- Be prepared for high rates (in short time bursts) in case a SN is behind the corner