

UNIVERSITÉ
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Overview of JUNO Large PMT Electronics

Jun Hu

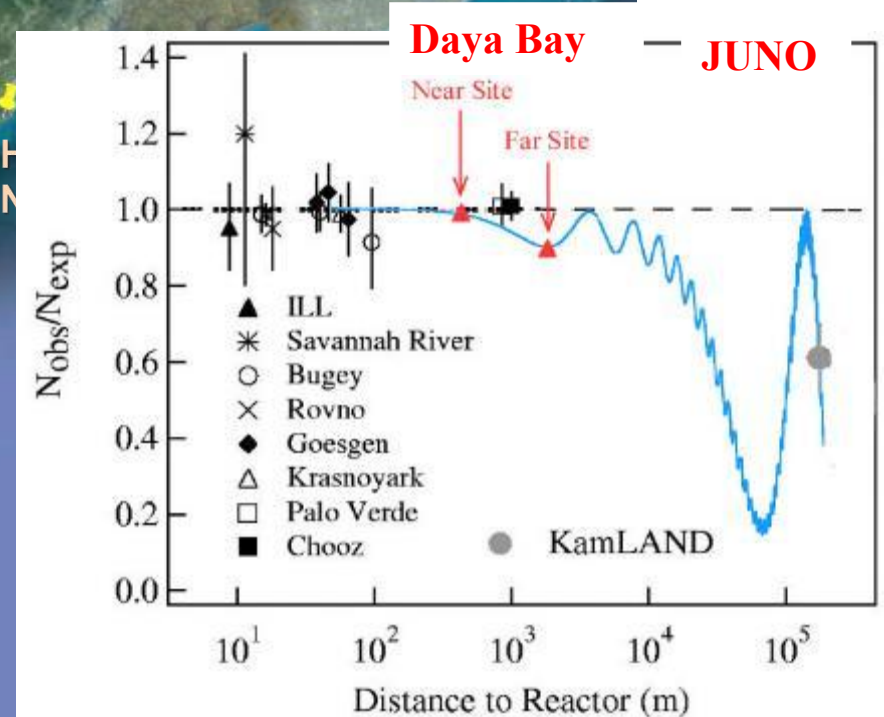
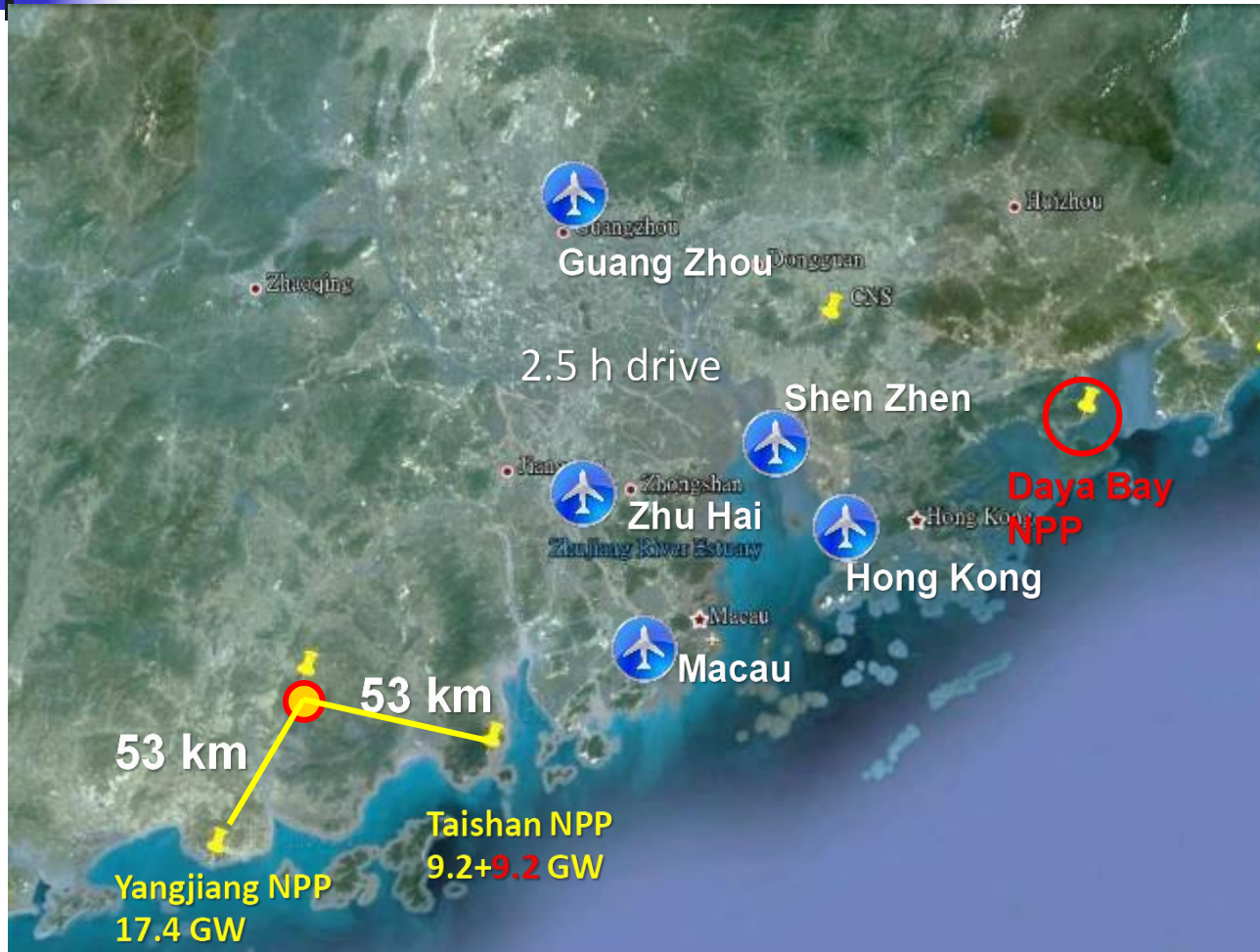
On behalf of the JUNO Collaboration

Institute of High Energy Physics, Beijing, China

Physics Opportunities of Large Liquid Scintillator Detectors

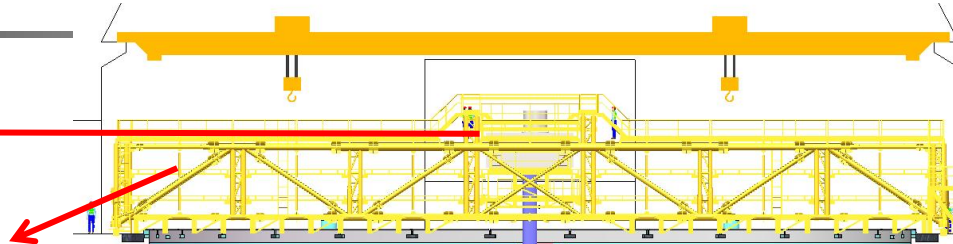
Oct 14, 2026

Jiangmen Underground Neutrino Observatory

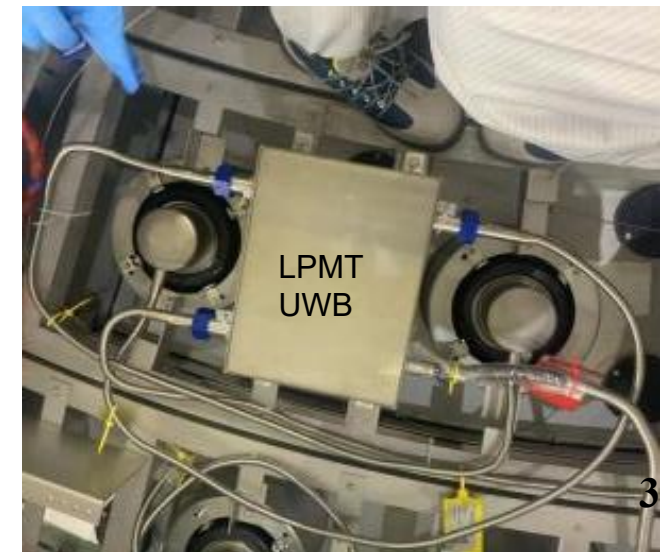


The JUNO Detector

Calibration house

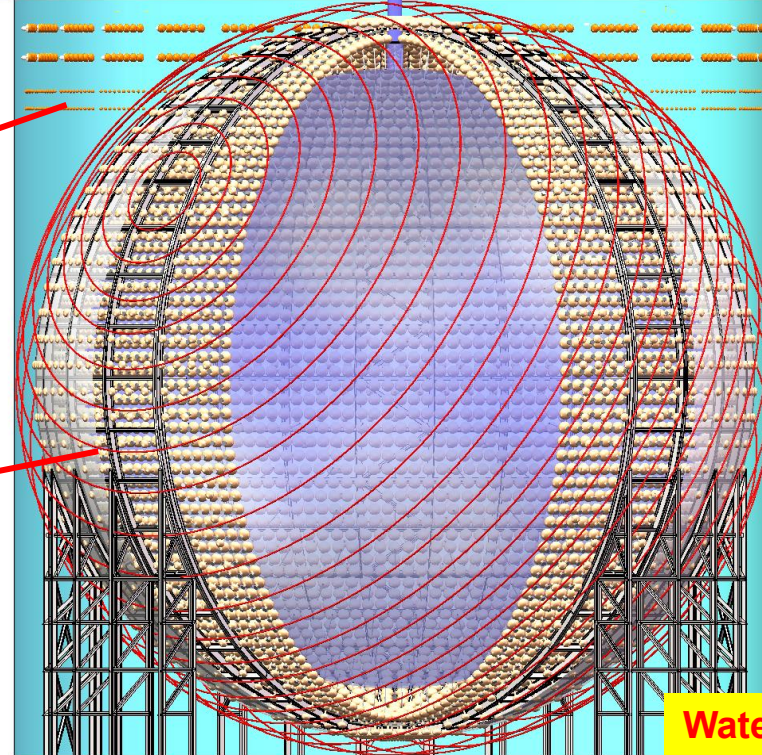


20" PMT



Water pool

- diameter 43.5m
- depth 44m



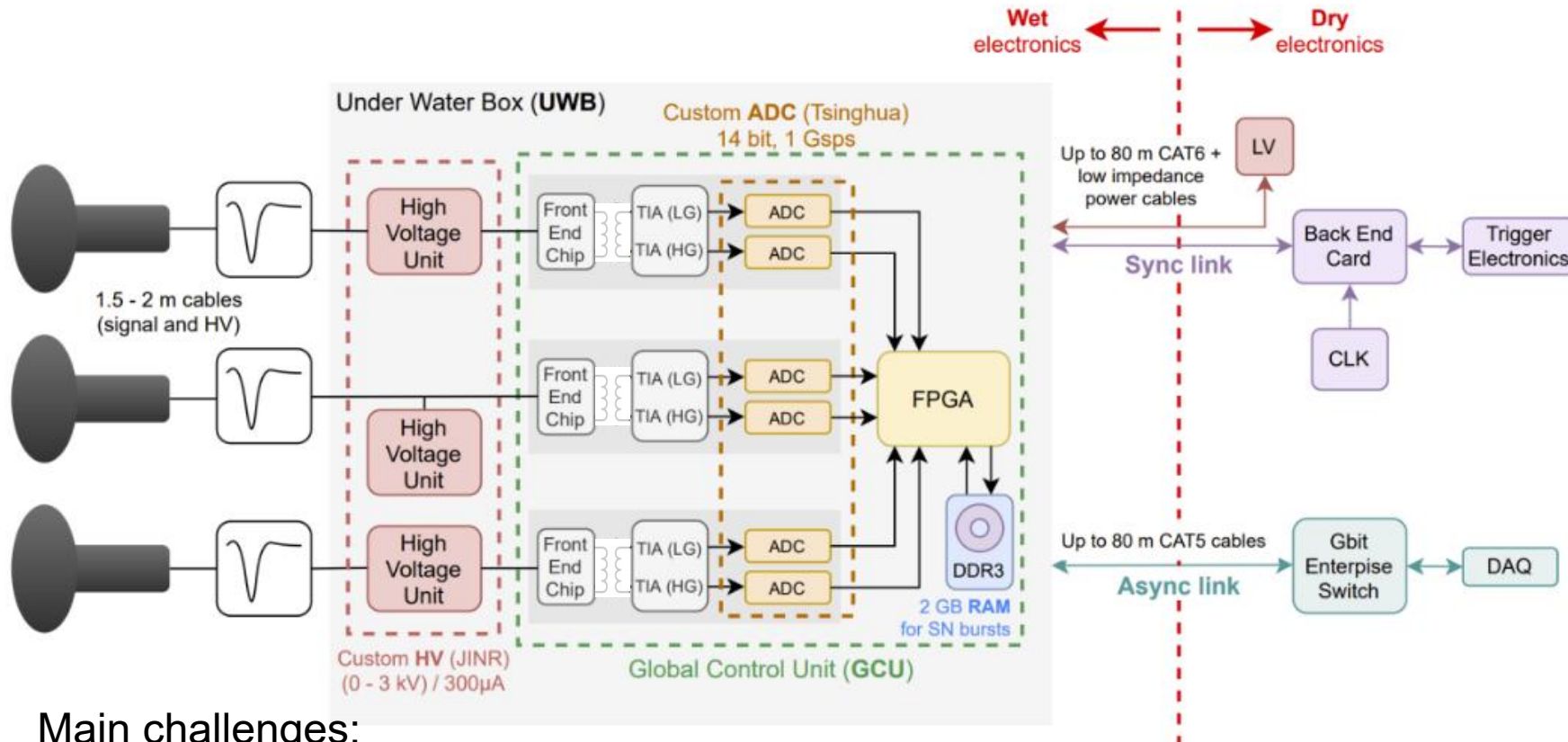
VETO system

- Top Tracker: plastic scintillator
- Water + 2400 20" PMT + 348 20" spare PMTs + 600 8" PMTs from Daya Bay
- Earth Magnetic Field shielding coils

Central detector

- Steel structure
- Acrylic sphere + 20kt Liquid scintillator
- 17612 20" PMT + 25600 3" PMT

Electronics Design



LPMT Under Water Box



Dry electronics in the electronics rooms

- DAQ switches,
- Back-End Card (BEC),
- Low-voltage power supply (LV).
- Trigger & Clock system

- Main challenges:
 - **Excellent energy resolution:** 10% @ 1-100 pe, 1% @ >100 pe
 - **Large dynamic range:** 1-4000 pe (7.5mV-7.5V)
 - **Huge number of channels:** ~20,000 LPMT channels
 - **Aerospace-grade reliability :** < 0.5% underwater electronics failure over 6 years

Under Water Box

PCB ,cable,
connector

Cooling

Waterproof

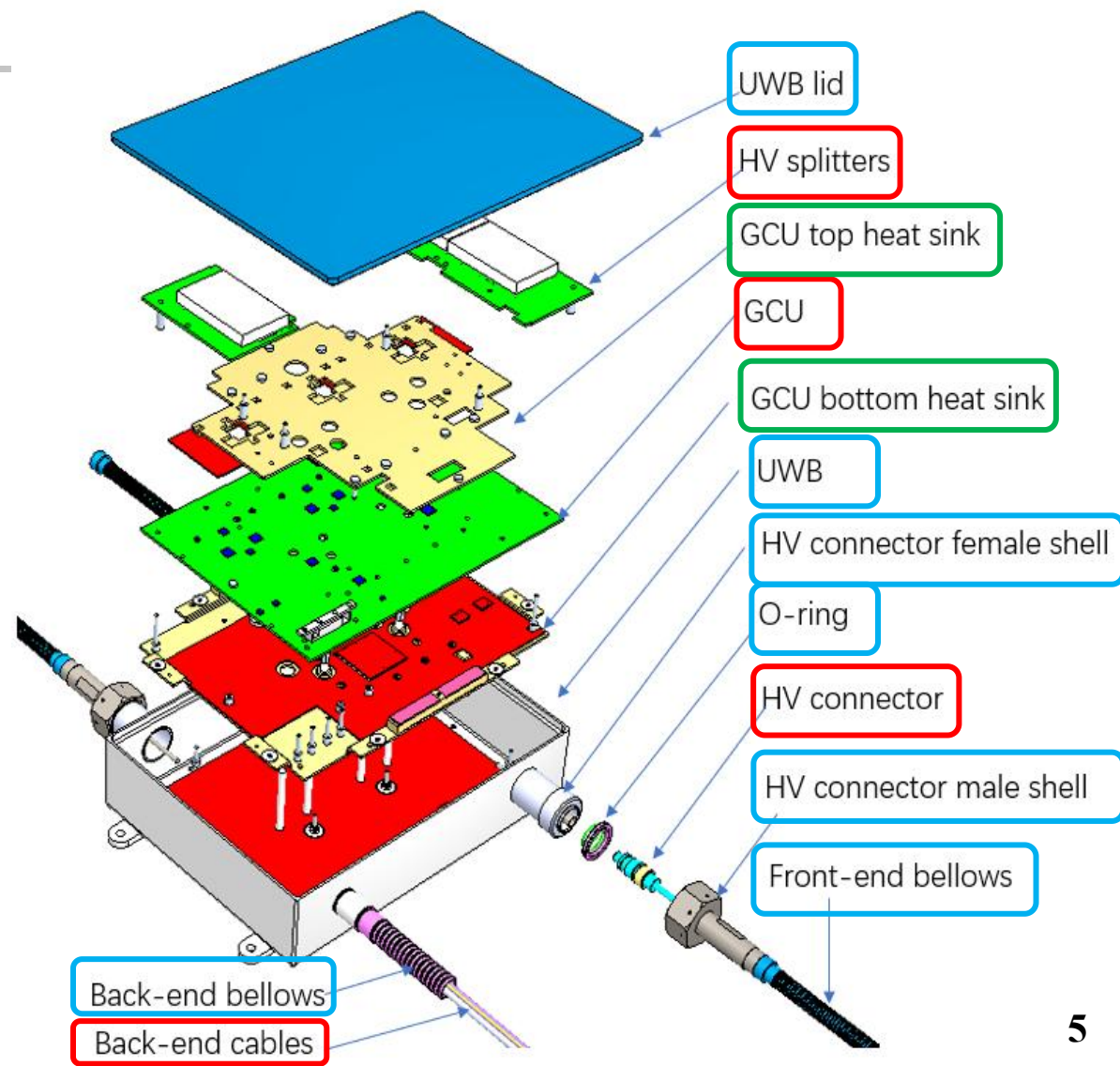
Bellow to PMT

Bellow to Dry electronics



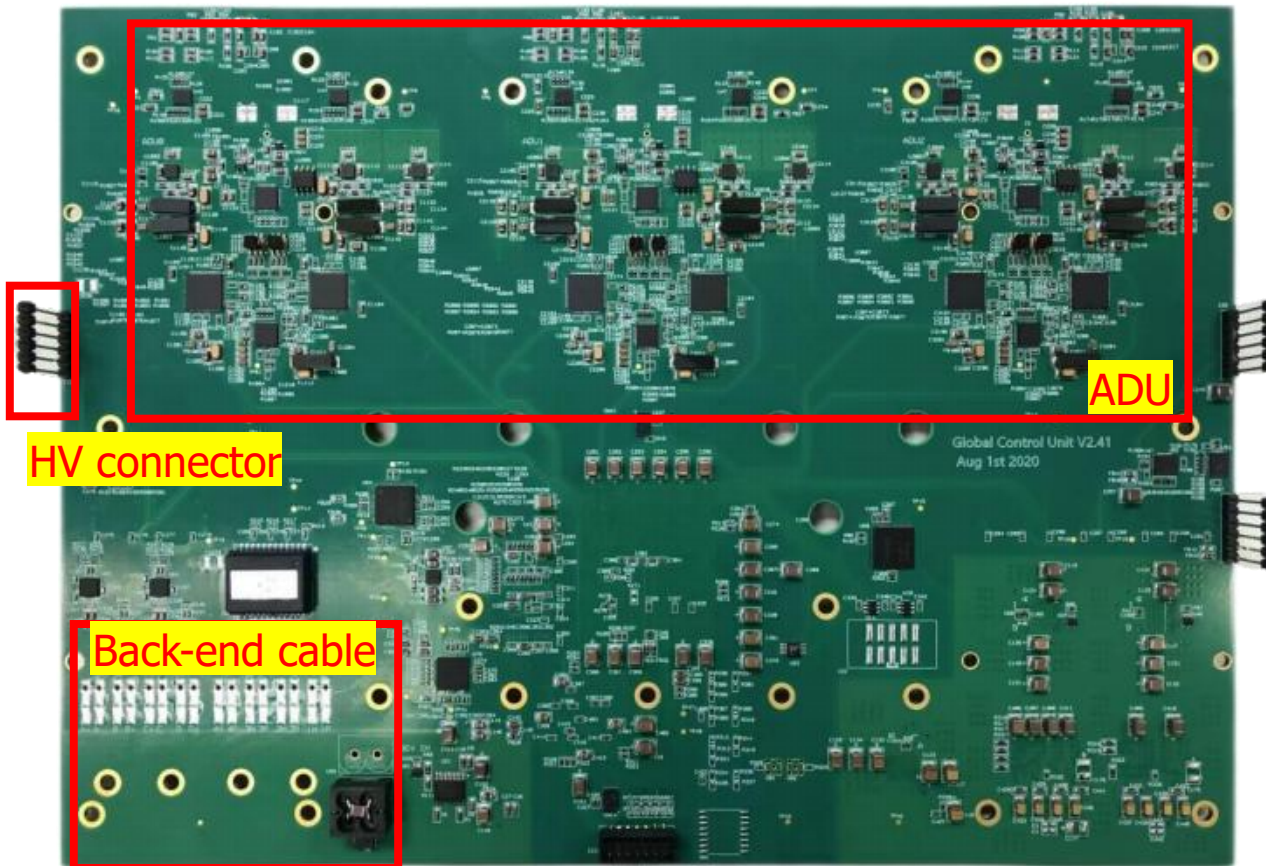
Bellow to PMT

Bellow to PMT

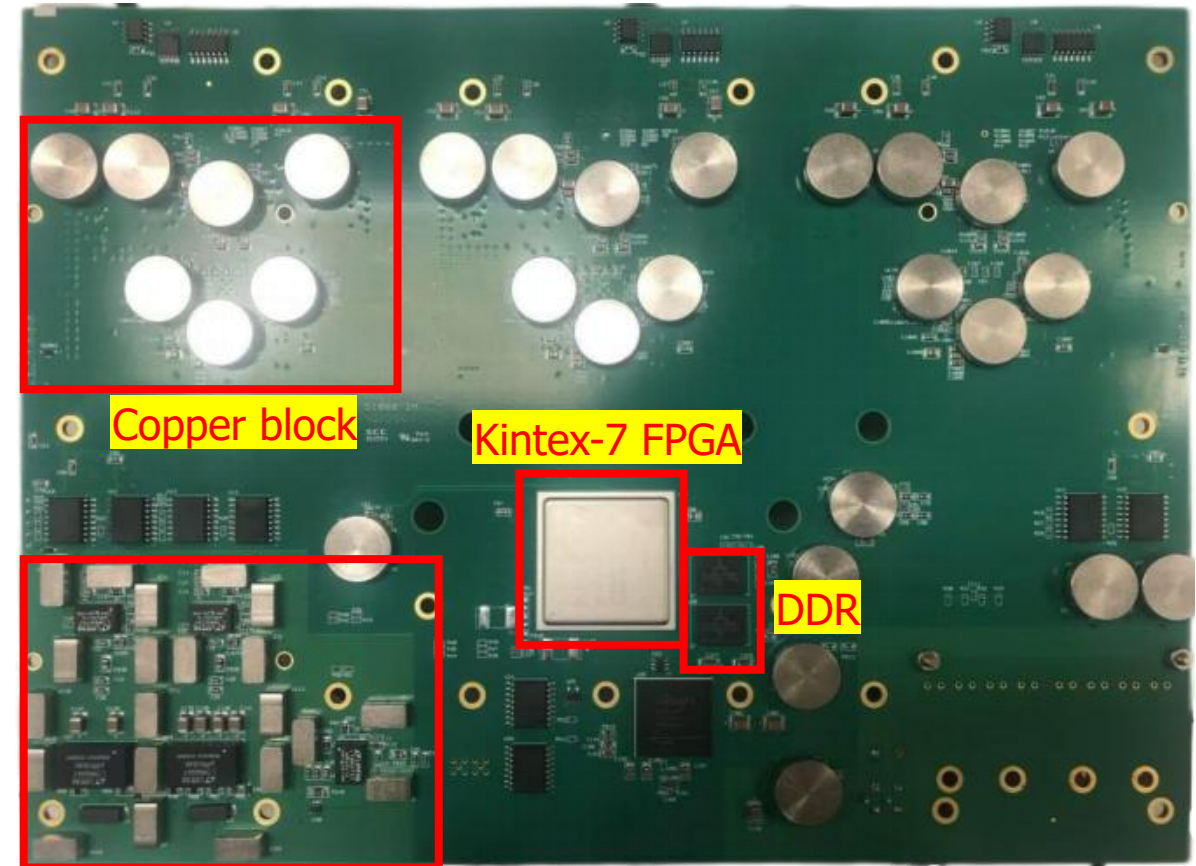


Global Control Unit (GCU)

By Univ. of Padova , INFN & IHEP

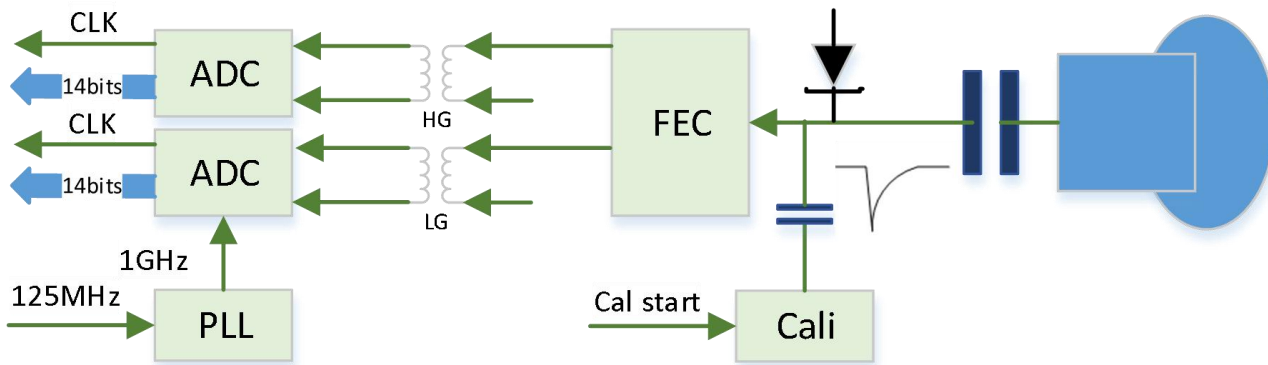


Component side

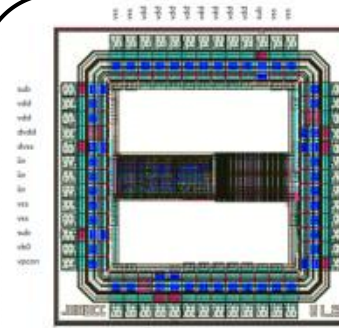


Cooling side

Analog-Digital Front-end Unit (ADU)



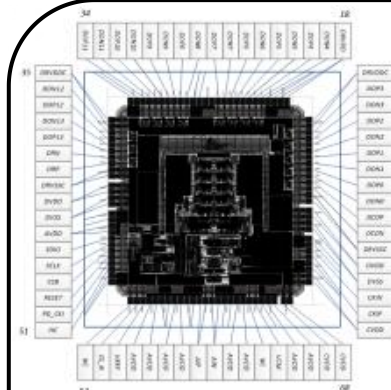
- Dynamic ranges:
 - Low Gain(8:1): 0~7.5V(4000pe)
 - High Gain(1:1): 0~960mV(128pe)
- Dual channels 1Gsps FADCs.
- Energy resolution: 0.1pe@1-100pe, 1%@>100pe
- Adjustable self-test pulse injection
- Over-voltage protection by circuit and FEC chips itself.



By IHEP

FEC: A current amplifier ASIC

- Package: QFN40 (5mmX5mm)
- Consumption: 100mW
- Range: 1, 1/8
- Noise (RMS): < 3.2uA (0.023pe)
- Input impedance: 1.1 Ω @10MHz

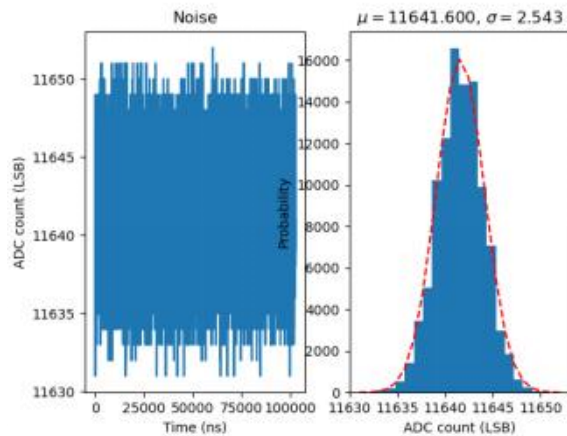


By Tsinghua Univ.

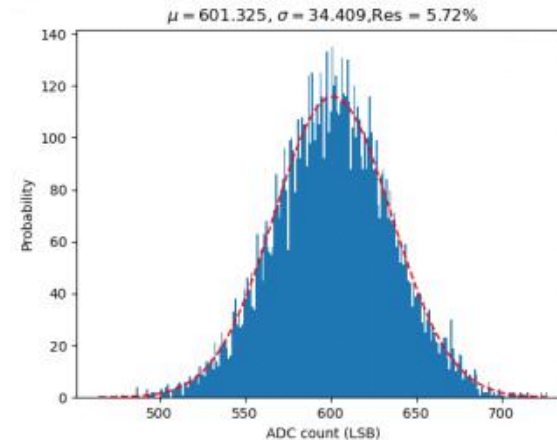
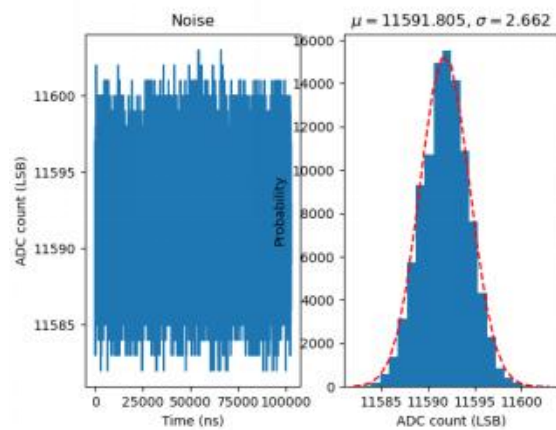
FADC:

- 12bit, 1GSPS
- ENOB of 10 @ fin up to 200MHz @ 1GSPS (-1.0 dBFS)
- SFDR = -68 dBc @ fin up to 200MHz @ 1GSPS (-1.0 dBFS)
- DNL < ± 0.5 LSB, INL < ± 2 LSB @12-bit level
- Power < 800mW

Front-end Performance

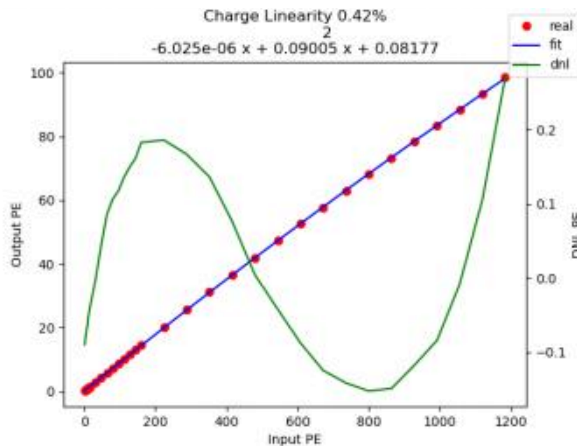


Noise

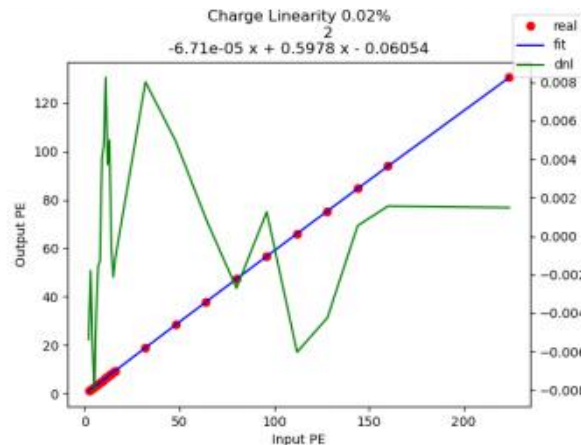


Energy Resolution

- **Noise:** < 400uV (SPE:7.5mV)
- **Linearity:** < 0.5%
- **Energy Resolution:** < 10%

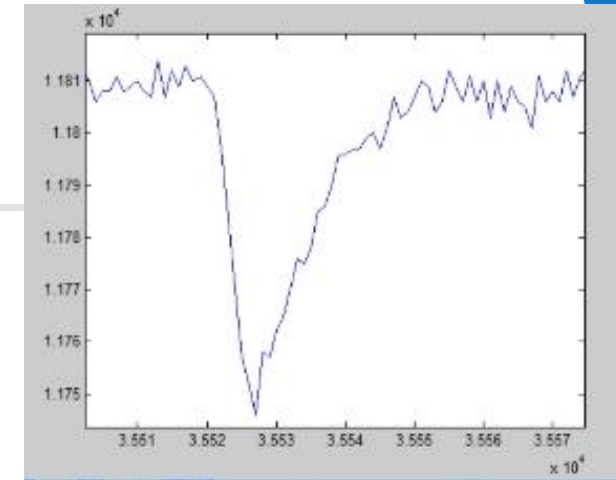
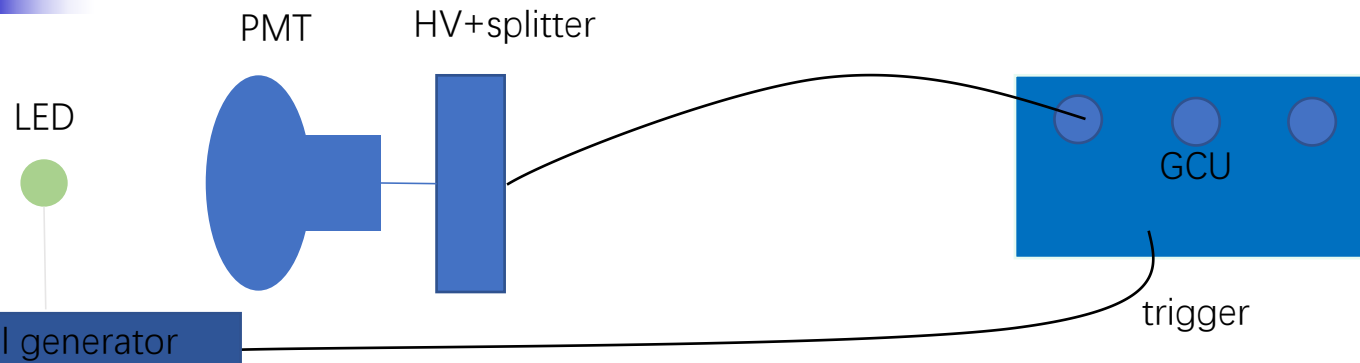


Linearity



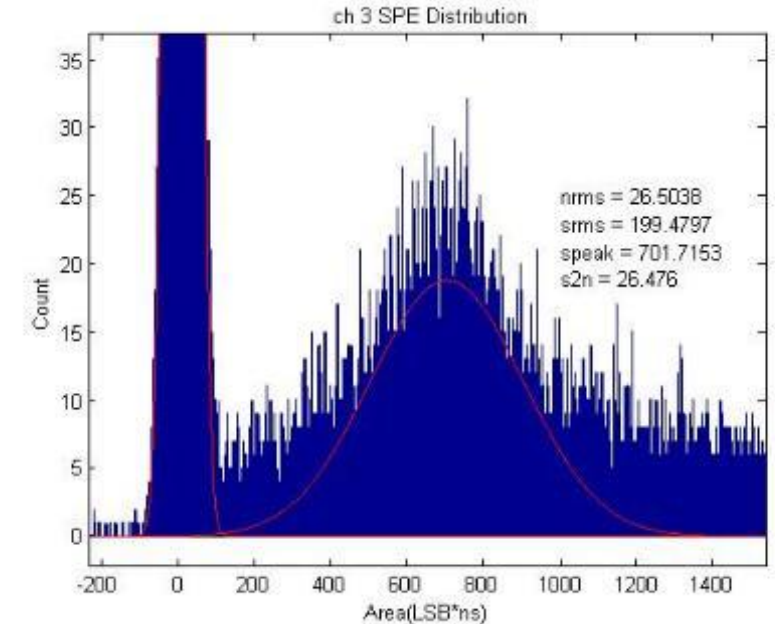
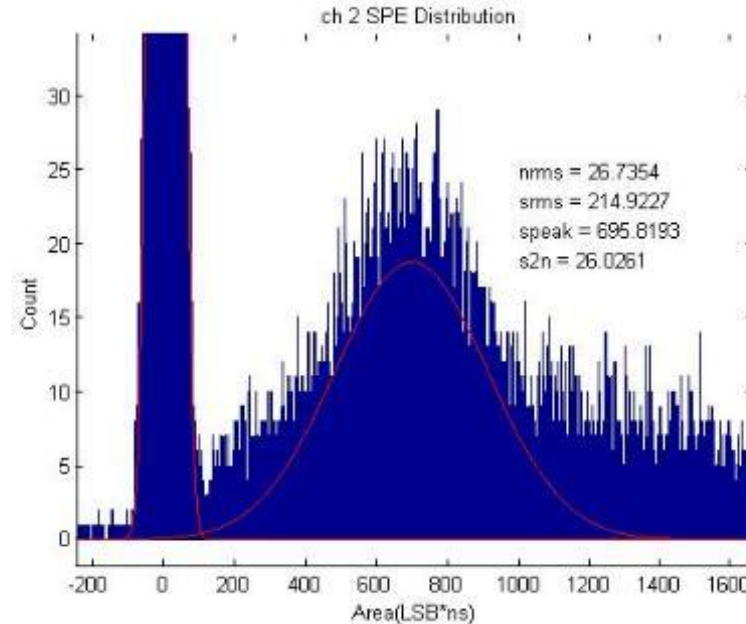
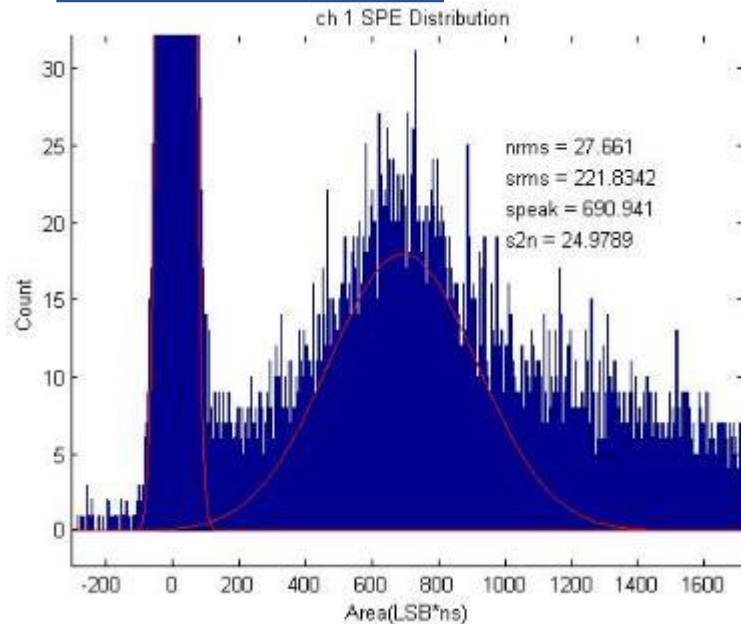
	CH1 LG	CH1 HG	CH2 LG	CH2 HG	CH3 LG	CH3 HG
Gain	0.079	0.54	0.078	0.54	0.078	0.53
Input noise (mV)	2.54	0.39	2.66	0.39	2.28	0.37
Linearity (%)	1.27	0.43	1.09	0.32	1.24	0.29
Energy Res (%)	0.38@ 100pe	6.81@ ~1pe	0.35@ 100pe	5.77@ ~1pe	0.4@ 100pe	5.76@ ~1pe

SPE Distribution Test



Typical SPE waveform (LPMT) ~ 70 ADC LSB

Signal to Noise rate > 20



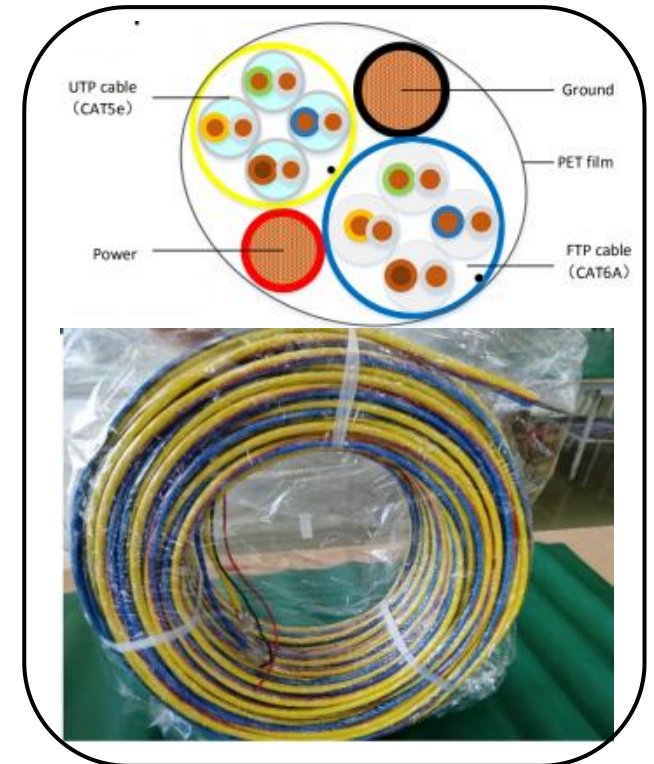
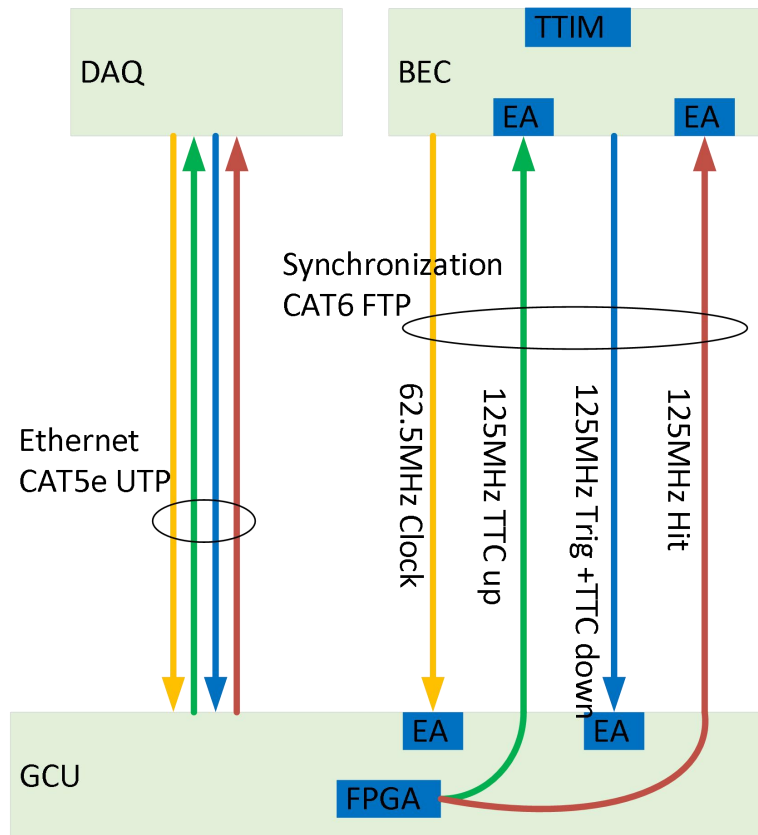
Back-end Transmission

■ CAT6 FTP - synchronization

- The FPGA drives signals onto the cables
- Cable Equalizer receives the signals from the cables
- Synchronized 62.5MHz clock fan-out to GCUs
- Real-time Hit information upload to TTIM
- TTC protocol transmits real-time global trigger and 1588 protocol for clock alignment

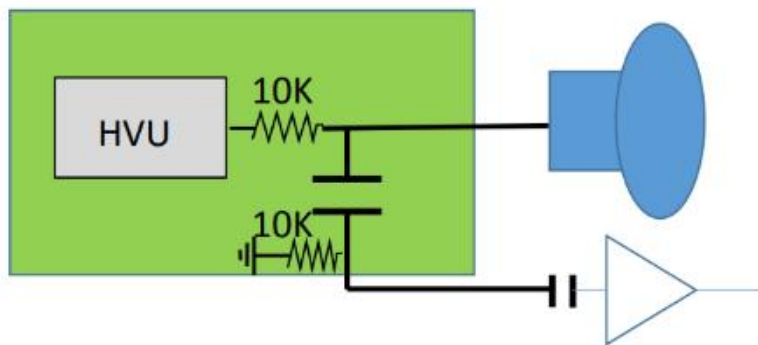
■ CAT5e UTP - Ethernet readout

- IPBUS&TCP protocol on FPGA
- RGMII interface to PHY



HV Splitter

(By IHEP)

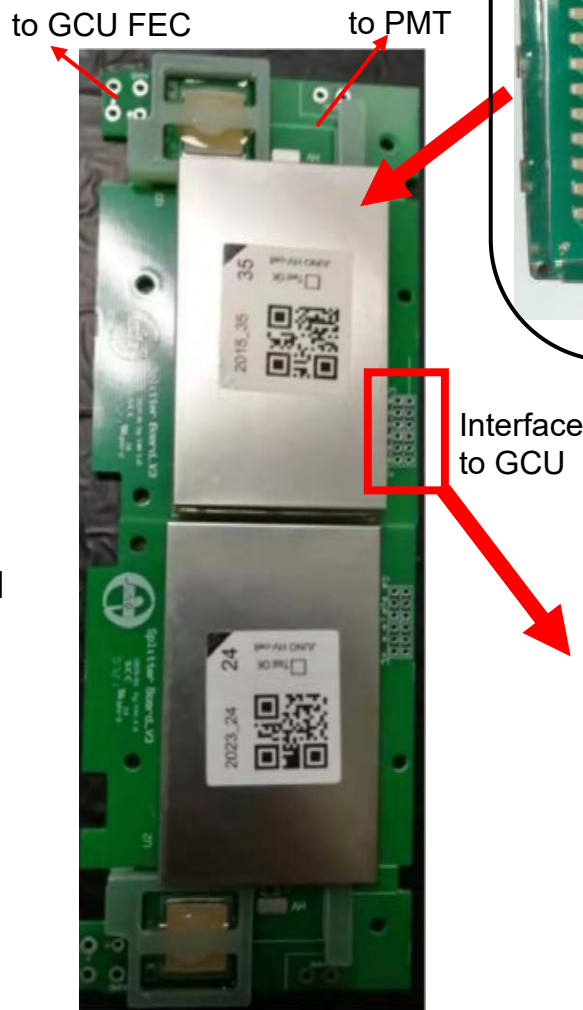


Function

- Serve as a motherboard for the HVU and distribute the high voltage to the PMT,
- Decouple the DC high voltage from the AC signal of interest for read-out.

Requirement

- Noise < 0.1pe
- HV withstanding > 2000V



Splitter of 2 channels



HVU (by JINR)

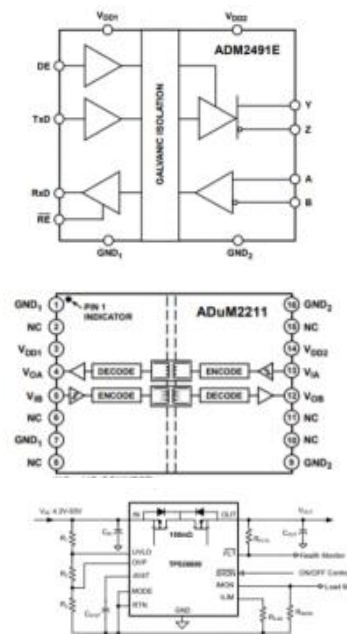
High Voltage Unit (HVU)

- Range of HVU is 800V-3000V in steps of ~0.5V.
- Ripple: 10 mVpp
- HV long term stability: 0.05%
- Temperature coefficient: 100 ppm/ °C
- Maximum output current: 300 μ A

RS485

Status
flag

24V



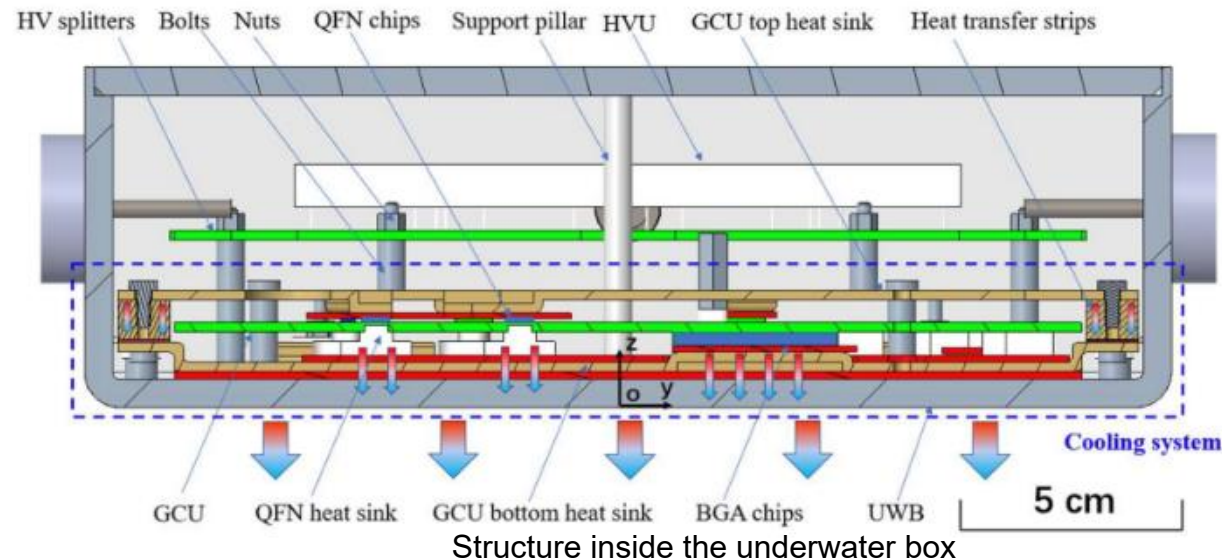
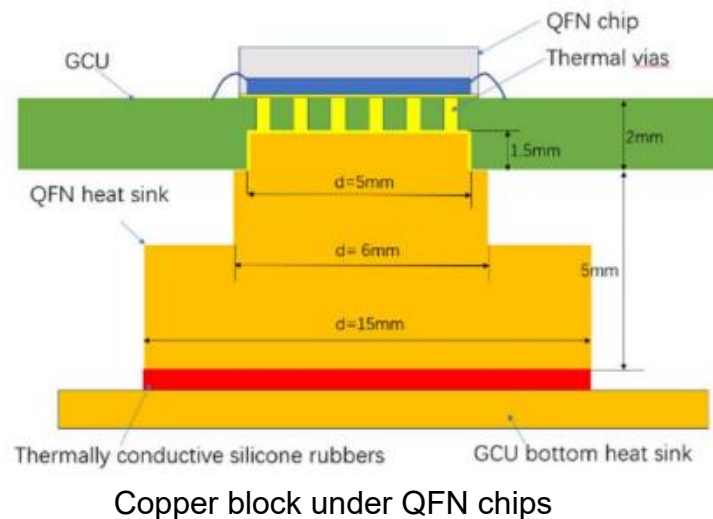
FPGA
on GCU

24VIN

Isolator for HV signal and PW on GCU side

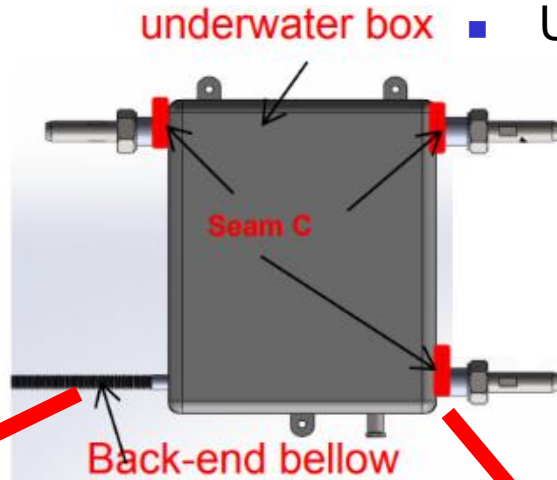
Cooling Mechanical Design

- Goal: Keep the component case temperature below 30°C (at ~25W dissipation, 22°C ambient)
- Features:
 - The bottom side of PCB serves as the primary heat transfer path.
 - BGA chips on the bottom side transfer heat through the their top.
 - QFN chips on the top side transfer heat via the copper block under the chips.
 - Additional copper blocks are placed close to DC-DC converters to aid in heat dissipation.



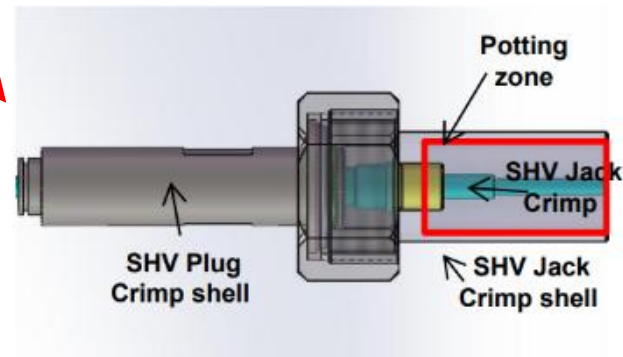
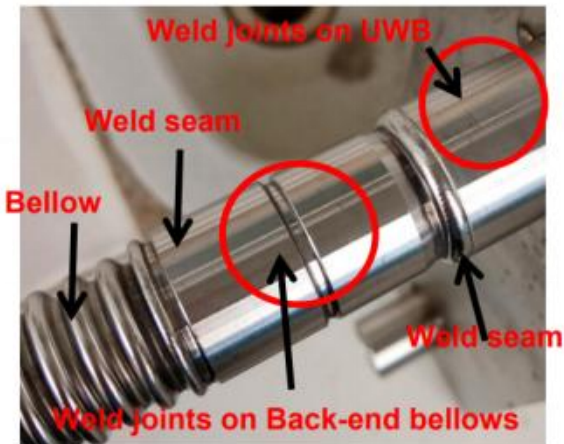
Waterproof Design

- UWB fitted with a 60m-90m back-end bellow, sealed by argon-arc welding.



- UWB and its lid sealing by laser welding

- UWB with 3 HV connector female shell by argon arc welding.



- HV connector shell sealing by 3 O-rings.

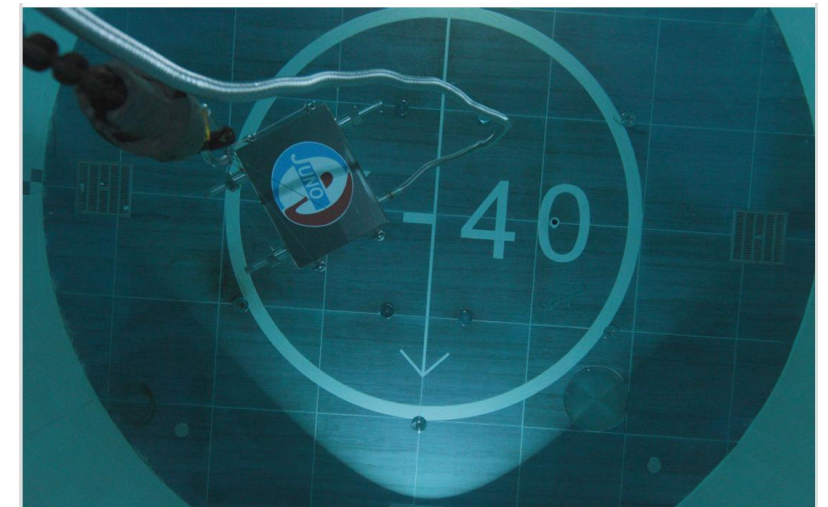


underwater box with long bellows

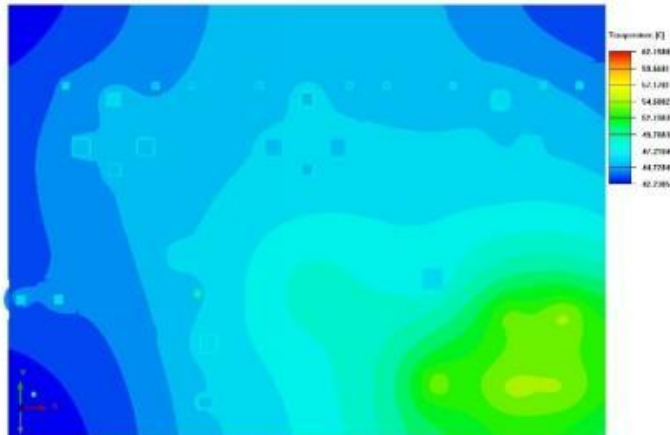
Under Water Test



Water tank in IHEP



40m swimming pool in Italy



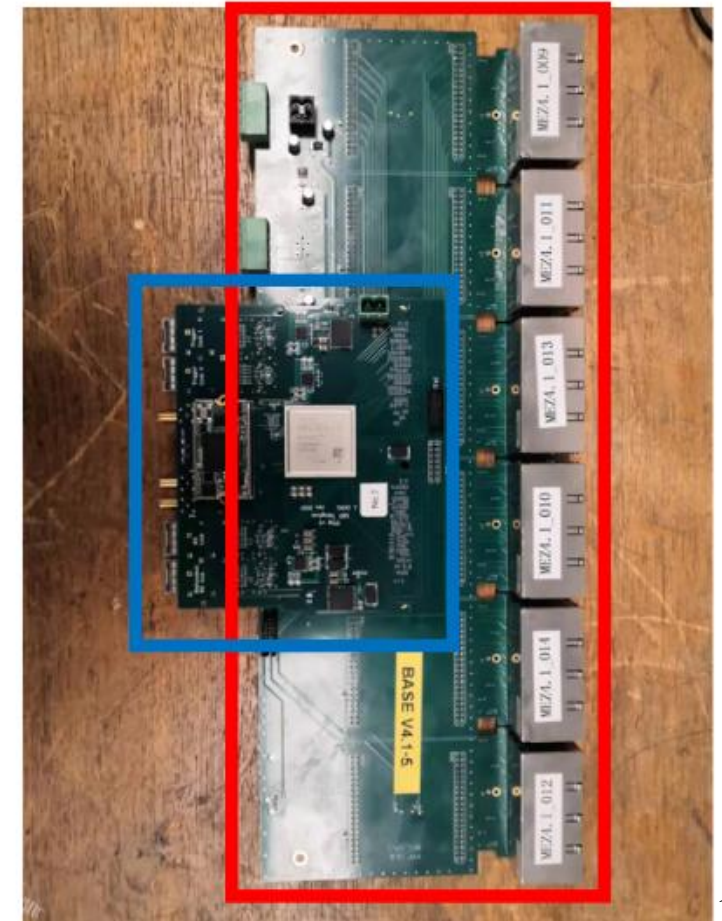
GCU temp. distribution (CFD simulation)

Tca(case-to-ambient)	DC-DC	Jitter cleaner	ADC	FEC	LDO
In 19.2°C air	28.6	26.6	26.5	26.6	26.9
in 20.5°C water	6.0	6.9	6.4	5.9	5.9

All chips remain below **30 °C** in 20.5°C water

Back-End Card (BEC)

- The Back-end Card connects the GCUs to the trigger electronics via CAT6 cables.
- Red box: Base board receives 48 Ethernet cables from the underwater boxes. (By Univ. Libre de Bruxelles)
- Blue box: Trigger/Timing interface mezzanine (TTIM) that distributes the CLK signal to GCUs and transfers the TRG signal between Global Trigger and GCUs. (By Tsinghua Univ.)
- Synchronous link: fixed latency link. Timing and trigger control (TTC) protocol. Nominal link speed 125 Mbps.





- 160 BECs
- 8 RMUs.
- 1 CTU.
- 2 Calibration Interface Box (CIB) in racks with clean ground.
- 5 GU for MM trigger system in MM racks.

- 12 WRS needed in the Electronics room
- 1 Atomic clock with GPS and WRS-GM installed in the Ground Control Room, provide NTP service.

Integration Test



IHEP, Beijing

- Using this test setup, we performed comprehensive batch testing
- Several critical issues, including back-end crosstalk and DDR-related EMI noise, were successfully resolved.



Padova, Italy



Zhongshan Container

- During PMT production, our readout electronics were deployed for PMT performance characterization and demonstrating superior performance.



Production of UWB (2020-2021)

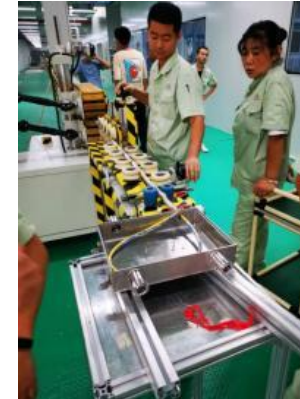
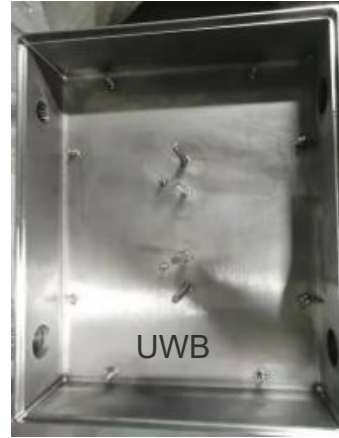


GCU module after assembly



Burn-in (aging) test

- Every manufacturing step is validated by meticulous electrical testing, complemented by strict leak checks, to guarantee the reliability of all modules delivered to the JUNO site.



Cable threading



Long term stability test



Assembly in box



Leak check

LPMT Electronics Installation (2022-2024)



Transportation to underground



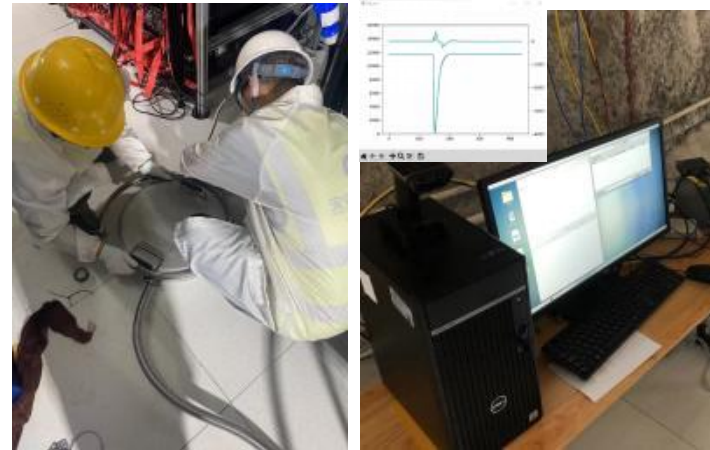
Nitrogen room



Connected to racks in
Electronics room



Installation on the steel structure



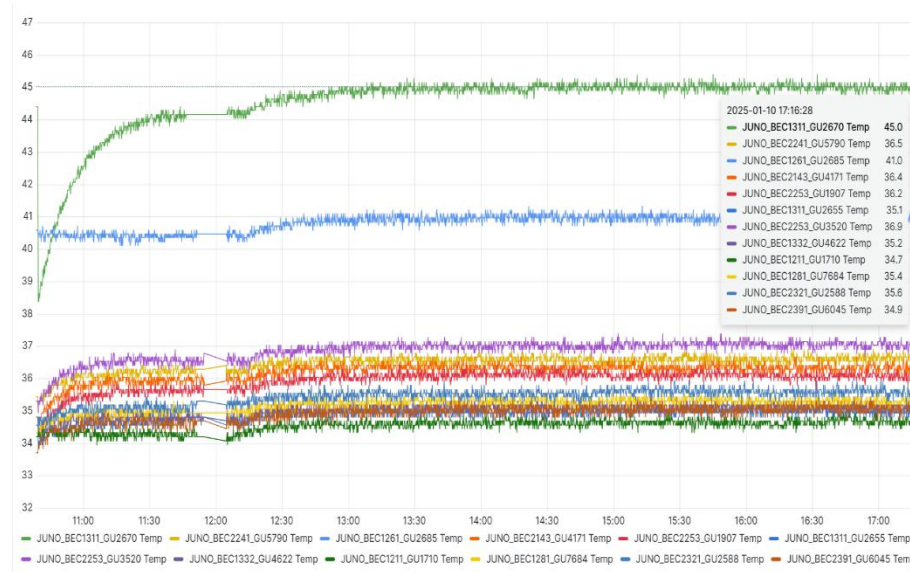
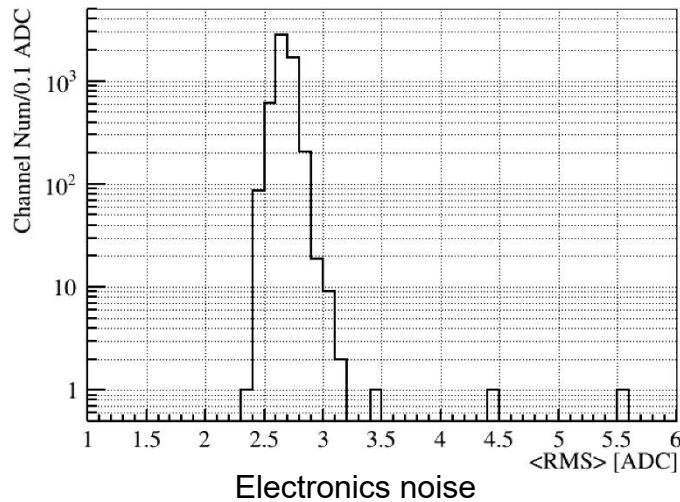
Leak check and refraction test

6797 UWBs installed

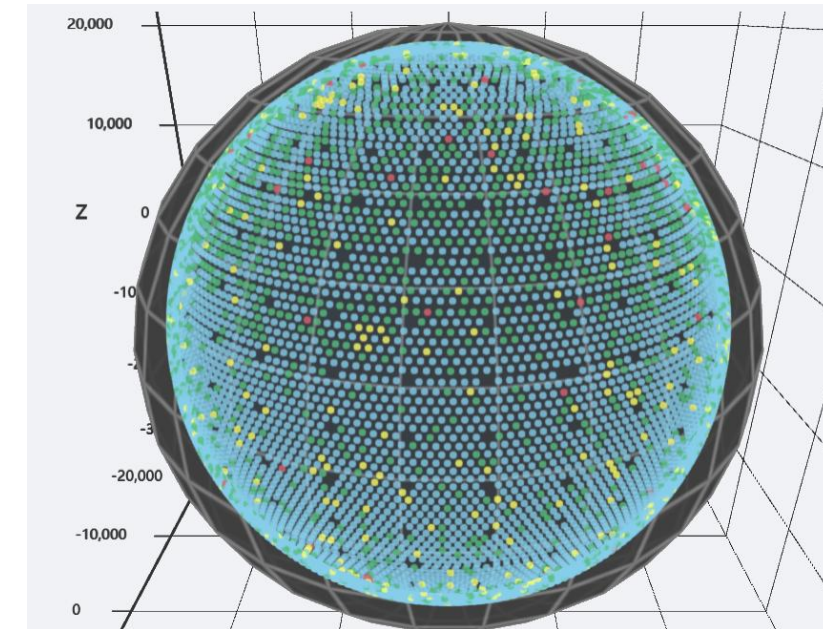
- CD : 5878
- VETO : 803
- ATMO : 116

Commissioning (2024-2025)

- We have already test all the UWBs underwater with PMTs
 - All electronics are alive.
 - Electronics noise is **~2.8 ADC** LSB in average, **4% of SPE** amplitude, consistent with our self-test results.
 - Most UWB maintain a temperature below 35°C, a few exceed this, and only 2 reach 40 °C.
 - The HVU works well and the DCR can be monitored online.



The highest 20 temperature UWBs

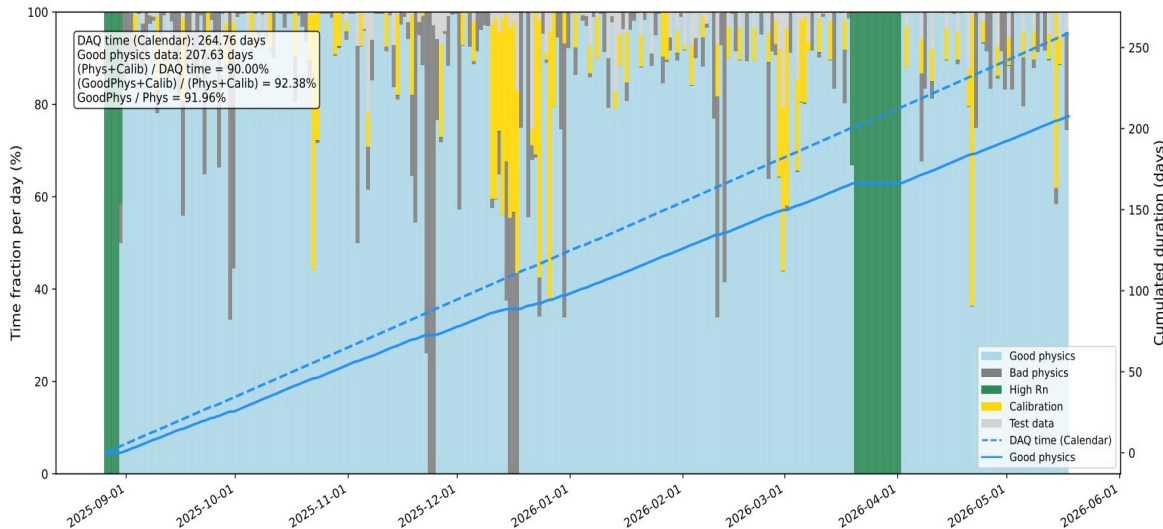


DCR monitoring

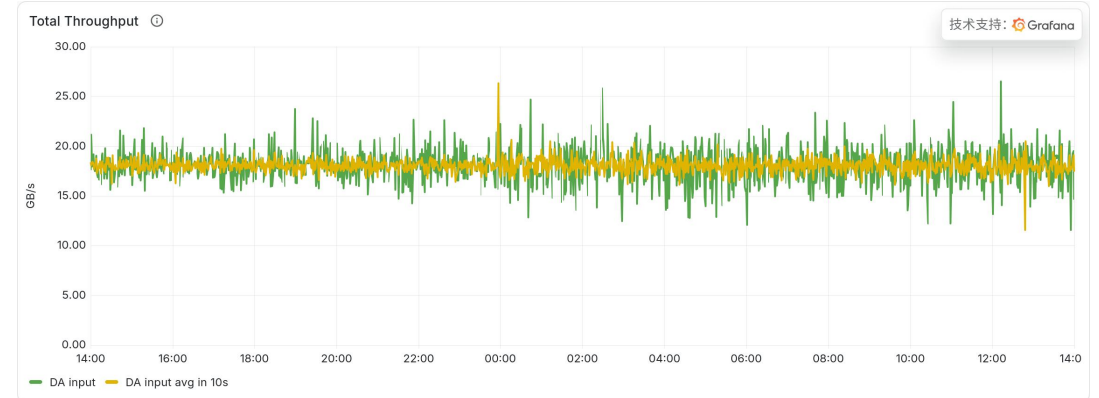
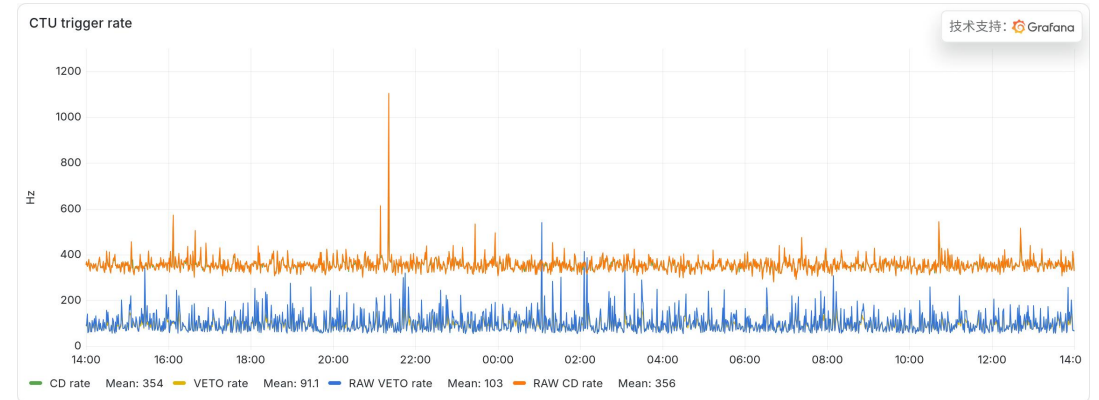
Operation Status

■ Electronics data taking status

- Detector electronics: 6792 GCUs, 100% enabled
- Readout bandwidth: $\approx 19.7 \text{ GB/s}$ ($WF \approx 15.0 + TQ \approx 4.7$)
- Triggers: CTU CD $\approx 353 \text{ Hz}$; VETO $\approx 91 \text{ Hz}$
- BEC data: send/recv $\approx 346 \text{ Hz}$ avg; hit $\approx 281 \text{ MHz}$ total

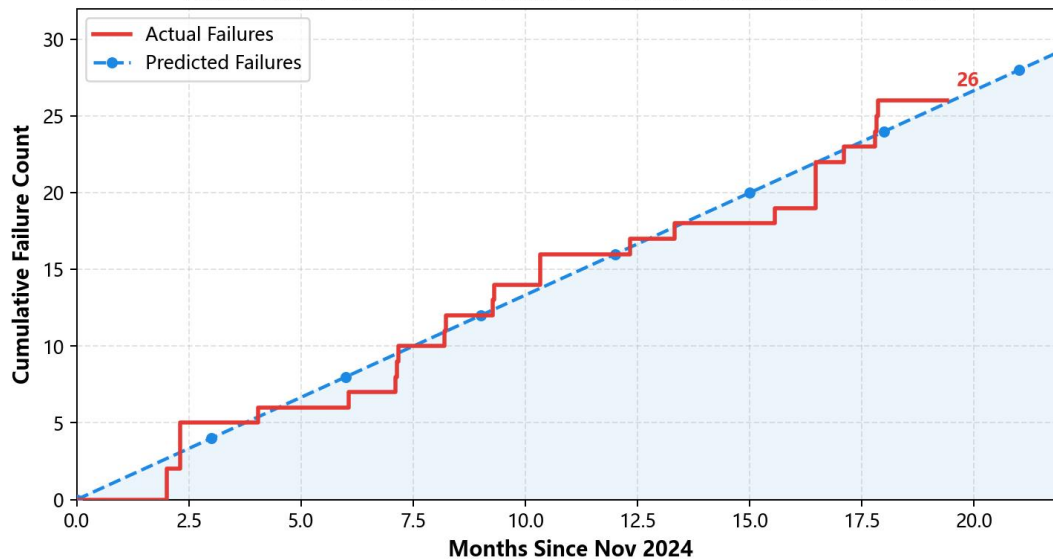


Reliable, high-performance electronics design ensures ultra-efficient physics data taking since August 2025



Failures Analysis

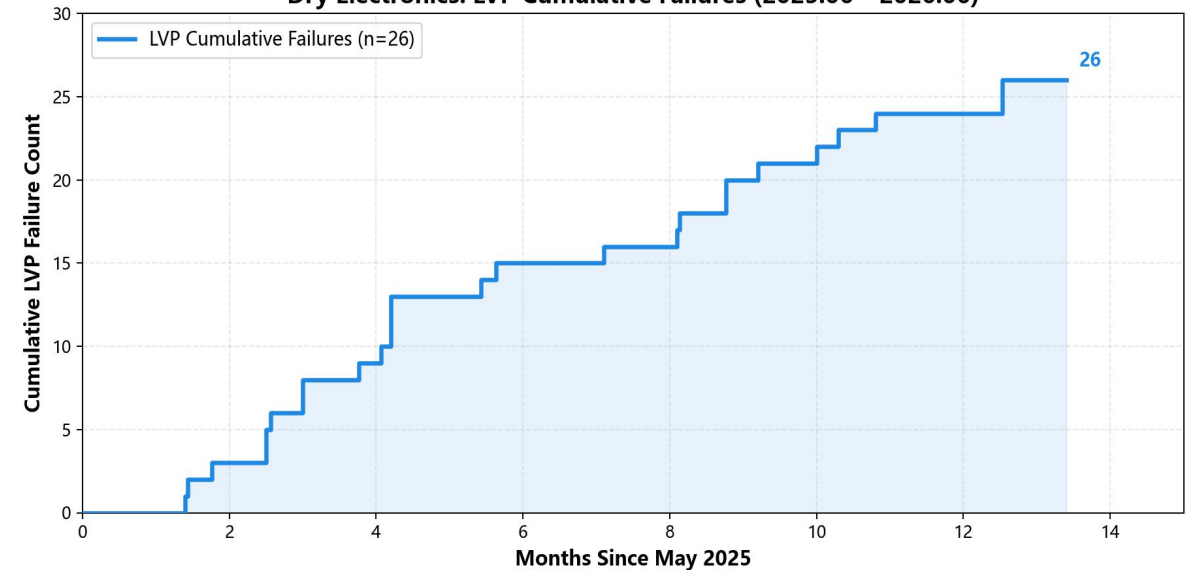
Underwater Electronics: Actual vs Predicted Cumulative Failures



UnderWater Box

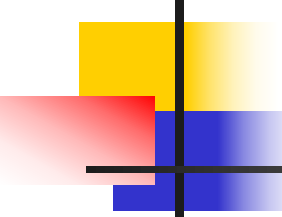
- Data range: 2024-11 ~ 2026-06 | 26 total failures across channels
- Failure curve matches reliability prediction — well within expectations.
- Top cause of failure: HV Module Damage (unstable output power).
- Only one instant water-ingress failure at the beginning.
- Only one UWB loss due to internal issue during operation.

Dry Electronics: LVP Cumulative Failures (2025.06 – 2026.06)



Dry Electronics

- LVP replacements 26 times: Trend ~2.0 LVP/month.
- BEC Back-End Cards: 5 replacements.
- UPS: Rm2 UPS PSU module damaged, on-site engineer repair.
- CTU: Internal fan failure, added external cooling fan.

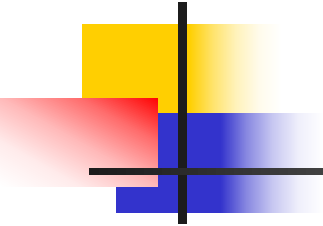
A decorative graphic on the left side of the slide, consisting of overlapping yellow, red, and blue squares with a black crosshair.

Summary

- Driven by JUNO's demanding scientific goals, the LPMT readout electronics must satisfy stringent performance requirements.
- Production and installation of the electronics have been completed with high yield.
- Detector performance validates that the electronics operate as designed.



Thank you !

A decorative graphic in the top left corner consisting of overlapping yellow, red, and blue squares with a black crosshair.

BACK UP

LPMT electronics group



Main Electronics Components

Core ASIC

Underwater Box

High-Voltage Module

Dry Electronics

Design Institutes

IHEP ; Tsinghua University

IHEP; University of Padova, Italy

Joint Institute for Nuclear Research, Dubna, Russia

Tsinghua University; University Libre Brussel, Belgium

Electronics Manager :

- Xiaoshan Jiang from IHEP,
- Alberto Garfagnini from University of Padova and INFN